REMARKS

At the outset, Applicants thank the Examiner for examining the pending application. The Office Action dated February 05, 2008 has been received and its contents carefully reviewed.

Summary of the Office Action

Claims 5, 6, 18-20 and 22-31 are rejected.

The Office Actions rejects claims 5, 6, 18-20 and 27-31 under 35 U.S.C. 103(a) as being unpatentable over the Applicants' Admitted Prior Art (AAPA) and Nanno (US 6,909,413), and rejects claims 22-26 under 35 U.S.C. 103(a) as being unpatentable over the AAPA in view of Tsutsui (US 7,196,701).

Summary of the Response to the Office Action

Applicants have amended claims 18, 20 and 22 to further define the invention. No new matter has been added. Reexamination and reconsideration of the pending claims are respectfully requested.

Rejection Under 35 U.S.C 103(a)

Claim 5 is allowable over the cited references in that claim 5 recites a combination of elements including, for example, "supplying the power source voltage to digital circuit devices including a data driving circuit and a gate driving circuit".

Claim 18 is allowable over the cited reference in that claim 18 recites a combination of elements including for example, "wherein the power source voltage is supplied to the digital circuit devices".

Claim 27 is allowable over the cited reference in that claim 27 recites a combination of elements including for example, "supplying the first power source voltage and the second power source voltages to the digital circuit devices".

With respect to claims 5, 18 and 27, the Office Action stated that AAPA (Fig. 2) teaches supplying the power source voltage to digital circuit devices. However, in AAPA, a power source voltage supplied to digital circuit devices is a voltage (VCC: 3.3V) higher than 3.0V. Thus, AAPA discloses that a voltage higher than 3.0V is supplied to digital circuit devices.

However, in claims 5, 18 and 27 of the claimed invention, power source voltage having a voltage lower than 3.0V is supplied to digital circuit devices. Thus, as power source voltage having a voltage lower than 3.0V is supplied to digital circuit devices, power consumption and EMI are lowered.

In addition, Nanno fails to disclose this feature of the claimed invention.
None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicants respectfully submit that claim 5, 18 and 27 and claims 6, 19-20 and 28-31, which depend therefrom, are allowable over the cited references.

Claim 22 is allowable over the cited references in that claim 22 recites a combination of elements including for example, "the second power source voltage being used to process digital signal of the digital circuit devices and being at least lower than the first power source voltage".

With respect to claim 22, the Office Action stated that AAPA teaches the first power source voltage being used to process digital signal of the digital circuit devise, and supplying the first power source voltage and the third power source voltage to the digital circuit devices.

As claimed in claim 22 of the claimed invention, a first power source voltage corresponds to VCC (3.3V) of AAPA, and a third power source voltage corresponds to VDD, GMS, VGH, VGL and so forth. But, AAPA fails to disclose a second power source voltage of the claimed invention.

The second power source voltage of the claimed invention has a voltage (CVCC: lower than 3.3V) lower than the first power source voltage (VCC), and is used for processing digital signal of digital circuit devices.

Thus, as claimed in claim 22 of the claimed invention, a voltage used for processing digital signal of digital circuit devices is a second power source voltage (CVCC), not a first power source voltage (VCC) of AAPA. The indication of the Office Action is improper. Applicants respectfully submit that the indication of the Office Action is withdrawn.

In addition, the Office Action stated that Tsutsui teaches a second power source voltage. VDD2 of Tsutsui as indicated by the Office Action (Column 1, lines 45-46 and lines 60-63) is obtained by boosting an input voltage (VIN). Thus, VDD2 of Tsutsui is a voltage higher than the input voltage (VIN).

None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicants respectfully submit that claim 22 and claims 23-26, which depend therefrom, are allowable over the cited references.

Conclusion

In view of the foregoing, Applicants respectfully request entry of the amendments to place the application in clear condition for allowance or, in the alternative, in better form for appeal.

If there are any other fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-0310. If a fee is required for an extension of time under 37 C.F.R. § 1.136 not accounted for above, such an extension is requested and the fee should also be charged to our Deposit Account.

Respectfully submitted,

MORGAN, LEWIS & BOCKIUS LLP

By: _____
Wonjoo Suh
Reg. No. L0296

Dated: May 1, 2008

CUSTOMER NO. 009629
MORGAN, LEWIS & BOCKIUS LLP
1111 Pennsylvania Avenue, NW
Washington, D.C. 20004
Tel.: (202) 739-3000
Fax: (202) 739-3001